	Search Text
1	scan$6 same (defect$4 fault$5 short open short/open shorts/opens) and (wire conductor segment) with (width wide fat big large heavy) and @ad<"20040813"
2	rout$4 same (wire conductor segment line) same (width wide fat big large heavy) and scan$6 same (defect$4 fault$5 short open short/open shorts/opens) and @ad<"20040813"
3	rout$4 same (wire conductor segment line) same (width wide fat big large heavy) and scan$6 same (insert$4) and @ad<"20040813"
4	(insert$4) same (short open short/open shorts/opens latch$2 gate flip$6) and (rout$4 same (wire conductor segment line) same (width wide fat big large heavy)) and @ad<"20040813"
5	(insert$4) same (short open short/open shorts/opens latch$2 gate flip$6) and (rout$4 same (wire conductor segment line) same (width wide fat big large heavy)) and @ad<"20040813" and (dft design with for with test)
6	(insert$4) same (short open short/open shorts/opens latch$2 gate flip$6) and (rout$4 same (wire conductor segment line) same (width wide fat big large heavy)) and @ad<"20040813" and (hdl vhdl)
7	(insert$4) same (short open short/open shorts/opens latch$2 gate flip$6) and (rout$4 same (wire conductor segment line) same (width wide fat big large heavy)) and @ad<"20040813" and (synthesis)
8	(insert$4) same (short open short/open shorts/opens latch$2 gate flip$6) and (rout$4 same (wire conductor segment line) same (width wide fat big large heavy)) and @ad<"20040813" and (synthesis and netlist)
9	rout$4 same (wire conductor segment line) same (width wide fat big large heavy) same (pin port pad terminal) and @ad<"20040813" and (insert$4) same (short open short/open shorts/opens latch$2 gate flip$6)
10	rout$4 same (wire conductor segment line) same (width wide fat big large heavy) same (pin port pad terminal) and @ad<"20040813" and (insert$4) same (short open short/open shorts/opens latch$2 gate flip$6) and scan$6
11	scan$6 with insert$6 and scan adj chain and (plac$6 same rout$4 layout$4)
12	scan$6 with insert$6 and scan adj chain and (plac$6 same rout$4 layout$4) and rout$4 same (wire conductor segment line) same (width wide fat big large heavy) same (pin port pad terminal)
13	scan$6 with insert$6 and scan adj chain and (plac$6 same rout$4 layout$4) and (vhdl hdl synthesis)
14	scan$6 with insert$6 and scan adj chain and (plac$6 same rout$4 layout$4) and (vhdl hdl synthesis) and netlist
15	scan$6 with insert$6 and scan adj chain and (plac$6 same rout$4 layout$4) and (vhdl hdl synthesis) and netlist and (short open short/open shorts/opens defect$5 fault$4)
16	scan$6 with insert$6 and scan adj chain and (plac$6 same rout$4 layout$4) and (vhdl hdl synthesis) and netlist and (short open short/open shorts/opens defect$5 fault$4) and (wire conductor segment line) same (width wide fat big large heavy) same (pin port pad terminal)